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EXAMINER	
WARE, CICELY Q	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,472	BODENSCHATZ, JOHN	
	Examiner	Art Unit	
	Cicely Ware	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/14/2005 have been fully considered but they are not persuasive. In applicant's **REMARKS** applicant recites that Fig. 6 does in fact show "a phase locked loop for generating the first clock frequency using said second clock frequency". However examiner asserts that Fig. 6 shows the implementation the device used to create the first clock frequency. The second clock frequency (C1) is input into a feedback loop (block 601). However, the first clock frequency is generated at the output of an NCO (block 603), which is not apart of the feedback loop (block 601). There is no "looping" operation performed from the output of the NCO to the input of the feedback loop.

Specification

1. The disclosure is objected to because of the following informalities:

a. Pg. 12, line 1, applicant uses "Period". Examiner suggests using "period" for clarification purposes.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1-4, 6, 7, 25, 26-33, 34-52, and 53- 60 are rejected under 35 U.S.C.

112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

a. Claims 1-4, 6, 25, and 34-52 recite limitations such as "said demultiplexer comprising a phase locked loop for generating the first clock frequency using the second clock frequency", "means for determining the first clock frequency using said second clock frequency, said determining means including at least a digital phase locked loop", and "generating the first clock frequency using a digital phase locked loop and said second clock frequency". However, after reviewing the specification, it is the understanding of the examiner that the "phase locked loop" used to generate the first clock frequency in the claims is actually not a "phase locked **loop**". In particular, Fig. 6 shows the implementation the device used to create the first clock frequency. The second clock frequency (C1) is input into a feedback loop (block 601). However, the first clock frequency is generated at the output of an NCO (block 603), which is not apart of the feedback loop (block 601). There is no "looping" operation performed from the output of the NCO to the input of the feedback loop. Therefore, it would have been obvious to one skill in the art at the time the invention was made that the first clock frequency is not generated using a phase locked **loop,** rather the first clock frequency is generated using a feedback loop, half period calculator, and NCO, wherein the half-period calculator and NCO are separate from the feedback loop (the half period calculator and the NCO are not apart of the feedback loop).

b. Claims 26-33 and 53- 60 recite limitations such as "said demultiplexer comprising at least a second order feedback loop for generating the first clock frequency", "said demultiplexer comprising at least a second order feedback loop having a half period calculator circuit for generating the first clock frequency", "generating the first clock frequency using at least a half period calculator circuit and said second clock frequency', and generating the first clock frequency using at least a second order feedback loop and said second clock frequency". However, after reviewing the specification (particularly Fig. 6), it is the understanding of the examiner that the first clock frequency (F1) is generated at the output of the NCO (block 603) after processing by the second order feedback loop and the half period calculator, not just by simply implementing the second order feedback loop of the half period calculator.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 25, 34-39, 42-45, 48-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Pappas (US Patent 4,658,406).

(1) With regard to claim 1, Pappas discloses a system for generating a first clock frequency for a plurality of data bursts compressed in time, the system comprising: a transmitter for transmitting a composite stream using the data bursts clock at a second

clock frequency; and a receiver comprising a demultiplexer, said receiver for acquiring said composite stream, and said demultiplexer comprising a phase locked loop for generating the first clock frequency using said second clock frequency (col. 1, lines 33-45, col. 2, lines 3-8).

(2) With regard to claim 2, claim 2 inherits all the limitations of claim 1. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(3) With regard to claim 3, claim 3 inherits all the limitations of claim 1. Pappas further discloses wherein said demultiplexer outputs the data bursts at the first clock frequency (col. 1, lines 33-45).

(4) With regard to claim 4, claim 4 inherits all the limitations of claim 1. Pappas further discloses wherein said demultiplexer includes a FIFO circuit (col. 6, lines 37-53).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 25, 34-39, 42-45, 48-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pappas (4,658,406).

(1) With regard to claim 25, claim 25 inherits all the limitations of claim 1.

However Pappas does not disclose wherein said phase locked loop comprises a digital phase locked loop.

However examiner takes Official Notice that a digital phase locked loop is used for locking the signals fast and efficiently due to the digital technology instead of the analog technology.

Therefore it would have been obvious to one of ordinary skill in the art to use a digital phase locked loop for locking the signals fast and efficiently due to the digital technology.

(2) With regard to claim 34, see rejection of claims 1 and 25.

(3) With regard to claim 35, claim 35 inherits all the limitations of claim 34. Pappas further discloses means for forming said composite stream (col. 1, lines 33-45).

(4) With regard to claim 36, claim 36 inherits all the limitations of claim 35. Pappas further discloses wherein said forming means comprises transmitter (col. 1, lines 33-45).

(5) With regard to claim 37, claim 37 inherits all the limitations of claim 34. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(6) With regard to claim 38, claim 38 inherits all the limitations of claim 34. Pappas further discloses wherein said determining means outputs the data bursts at the first clock frequency (col. 1, lines 33-45).

(7) With regard to claim 39, claim 39 inherits all the limitations of claim 34. Pappas further discloses wherein said demultiplexer includes a FIFO circuit (col. 6, lines 37-53).

(8) With regard to claim 42, see rejection of claims 1, 25, and 34.

(13) With regard to claim 43, claim 43 inherits all the limitations of claim 42. Pappas further discloses transmitting said composite stream using the data bursts clocked at said second clock frequency (col. 1, lines 33-45).

(9) With regard to claim 44, claim 44 inherits all the limitations of claim 42. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(10) With regard to claim 45, claim 45 inherits all the limitations of claim 42. Pappas further discloses outputting the data bursts at the first clock frequency (col. 1, lines 33-45).

(11) With regard to claim 48, see rejection of claims 1, 25, and 34.

(12) With regard to claim 49, claim 49 inherits all the limitations of claim 48. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(13) With regard to claim 50, claim 50 inherits all the limitations of claim 48. Pappas further discloses outputting the data bursts at the first clock frequency (col. 1, lines 33-45).

6. Claims 6, 26-29, 40, 46, 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pappas (US Patent 4,658,406) as applied to claims 1, 25, 34, 42, 48, in view of Kovacs et al. (US Patent 5,495,512).

(1) With regard to claim 6, claim 6 inherits all the limitations of claim 25. However Pappas does not disclose wherein said digital phase locked loop comprises a second order feedback loop.

However Kovacs et al. discloses wherein said digital phase locked loop comprises a second order feedback loop. Kovacs et al. states that conventional second order feedback circuits are PLL's and may be digital, continuous time types, analog and discrete time types (col. 1, lines 19-21).

Therefore it would have been obvious to one of ordinary skill in the art to modify Pappas in view of Kovacs et al. to incorporate wherein said digital phase locked loop comprises a second order feedback loop in order to control the damping factor and the scaling factor along with possessing an effective size cost and simplicity (Kovacs et al., col. 1, lines 62-67 – col. 2, lines 1-5).

(2) With regard to claim 40, claim 40 inherits all the limitations of claim 34. See rejection of claim 6.

7. Claims 26-29, 46, 51, 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pappas (US Patent 4,658,406) as applied to claims 1, 42, 48, in view of Kovacs et al. (US Patent 5,495,512).

(1) With regard to claim 26, see rejection of claim 1. Pappas discloses all the limitations of claim 1. However Pappas does not disclose at least a second order feedback loop for generating determining a period of the first clock frequency.

However Kovacs et al. discloses at least a second order feedback loop for generating determining a period of the first clock frequency in order to control the damping factor and the scaling factor along with possessing an effective size cost and simplicity (Kovacs et al., col. 1, lines 62-67 – col. 2, lines 1-5). Kovacs et al. discloses wherein conventional second order feedback circuits are PLL's and may be digital, continuous time types, analog and discrete time types (col. 1, lines 19-21).

Therefore it would have been obvious to one of ordinary skill in the art to modify Pappas in view of Kovacs et al. to incorporate at least a second order feedback loop for generating determining a period of the first clock frequency in order to control the damping factor and the scaling factor along with possessing an effective size cost and simplicity (Kovacs et al., col. 1, lines 62-67 – col. 2, lines 1-5)

(2) With regard to claim 27, claim 27 inherits all the limitations of claim 26. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(3) With regard to claim 28, claim 28 inherits all the limitations of claim 26. Pappas further discloses wherein said demultiplexer outputs the data bursts at the first clock frequency (col. 1, lines 33-45).

(4) With regard to claim 29, claim 29 inherits all the limitations of claim 26. Pappas further discloses wherein said demultiplexer comprises a FIFO circuit (col. 6, lines 37-53).

(5) With regard to claim 46, claim 46 inherits all the limitations of claim 42. See rejection of claim 26.

(6) With regard to claim 51, claim 51 inherits all the limitations of claim 48. Kovacs et al. further discloses wherein conventional second order feedback circuits are PLL's and may be digital, continuous time types, analog and discrete time types (col. 1, lines 19-21).

(7) With regard to claim 57, see rejection of claim 26.

(8) With regard to claim 58, claim 58 inherits all the limitations of claim 57. Pappas discloses comprising transmitting said composite stream using the data bursts clocked at said second clock frequency (col. 1, lines 33-45).

(9) With regard to claim 59, claim 59 inherits all the limitations of claim 57. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(10) With regard to claim 60, claim 60 inherits all the limitations of claim 57. Pappas further discloses outputting the data bursts at the first clock frequency (col. 1, lines 33-45).

8. Claims 30-33, 53, 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pappas (US Patent 4,658,406), in view of Hulsing, II (US Patent 5,500,627).

(1) With regard to claim 30, claim 30 inherits all the limitations of claim 1. Pappas discloses all the limitations of claim 26. See rejection of claim 1.

However Pappas does not disclose a half period calculator circuit for generating at least one full cycle of the first clock frequency.

However Hulsing, II discloses a half period calculator circuit for generating at least one full cycle of the first clock frequency (abstract, col. 1, lines 15-67, col. 2, lines 1-4, col. 3, lines 2-8, 15-19).

Therefore it would have been obvious to one of ordinary skill in the art to modify Pappas in view of Hulsing, II to incorporate a half period calculator circuit for generating at least one full cycle of the first clock frequency in order to prevent the demodulator output from containing rectified information such as DC offset in addition to the desired AC signal information (Hulsing, II, col. 1, lines 33-40).

(2) With regard to claim 31, claim 31 inherits all the limitations of claim 30. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(3) With regard to claim 32, claim 32 inherits all the limitations of claim 30. Pappas further discloses wherein said demultiplexer outputs the data bursts at the first clock frequency (col. 1, lines 33-45).

(4) With regard to claim 33, claim 33 inherits all the limitations of claim 30. Pappas further discloses wherein said demultiplexer includes a FIFO circuit (col. 6, lines 37-53).

(5) With regard to claim 53, see rejection of claim 30.

(6) With regard to claim 54, claim 54 inherits all the limitations of claim 53. Pappas further discloses comprising transmitting said composite stream using the data bursts clocked at said second clock frequency (col. 1, lines 33-45).

(7) With regard to claim 55, claim 55 inherits all the limitations of claim 53. Pappas further discloses wherein said second clock frequency is higher that the first clock frequency (col. 1, lines 33-45, Fig. 4)

(8) With regard to claim 56, claim 56 inherits all the limitations of claim 53. Pappas further discloses outputting the data bursts at the first clock frequency (col. 1, lines 33-45).

9. Claims 7, 41, 47, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pappas (US Patent 4,658,406) in view of Kovacs et al. (US Patent 5,495,512), as applied to claims 6, 42, 51 in further view of Minoda et al. (US Patent 5,661,425).

(1) With regard to claim 7, claim 7 inherits all the limitations of claim 6. Pappas in combination with Kovacs et al. disclose all the limitations of claim 6. However Pappas in combination with Kovacs et al. do not discloses wherein said second order feedback loop comprises a half period calculator circuit.

However Minoda et al. discloses in (Fig. 23) wherein the PLL comprises a half period calculator circuit. (col. 3, lines 25-28, col. 10, line 41-47).

Minoda et al. does not explicitly disclose a second order feedback loop. However it is well known in the art that conventional second order feedback circuits are PLL's and may be digital, continuous time types, analog and discrete time types.

Therefore it would have been obvious to one of ordinary skill in the art to modify the inventions of Pappas in combination with Kovacs et al. in view of Minoda et al. to incorporate wherein said second order feedback loop comprises a half period calculator circuit reduces correction error by controlling a PLL clock signal in units of half period of master clock signal (Minoda et al., col. 10, lines 45-47).

(2) With regard to claim 41, claim 41 inherits all the limitations of claim 46. See rejection of claim 7.

(3) With regard to claim 47, claim 47 inherits all the limitations of claim 42.

(3) With regard to claim 52, claim 52 inherits all the limitations of claim 51. See rejection of claim 47. See rejection of claim 7.

(4) With regard to claim 52, claim 52 inherits all the limitations of claim 48. See rejection of claim 7.

Conclusion

10. The prior art made record of and not relied upon is considered pertinent to applicant's disclosure:

a. Bates US Patent 6,748,039 discloses a system and method for

synchronizing a skip pattern and initializing a clock forwarding interface in a multiple-clock system.

b. Gauthier et al. US Patent 6,784,752 discloses a post-silicon phase offset control of phase locked loop input receiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cicely Ware whose telephone number is 571-272-3047. The examiner can normally be reached on Monday – Friday, 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Cicely Ware

cqw
January 23, 2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER